ATTACHMENT A

Substitute Specification (clean copy)

MONITORING THE REDUCTION IN THICKNESS AS MATERIAL IS REMOVED FROM A WAFER COMPOSITE AND TEST STRUCTURE FOR MONITORING REMOVAL OF MATERIAL

Cross-Reference To Related Application(s)

[0001] This application is a U.S. National Phase of International Application No. PCT/DE2004/000801, filed April 16, 2004, which claims priority to German 103 17 747.7, filed April 17, 2003. The entire contents of all the above-identified applications are incorporated herein by reference.

Field of Invention

[0002] The invention relates to the above-specified technical field in the context of manufacturing semiconductor wafers from two single connected wafers that are bonded together. More particularly, the invention relates to a method for monitoring the reduction in thickness of a wafer pair and a test device (test structure) provided at or in the wafer itself to enable the monitoring of the material removal.

Background of the Invention

[0003] US 6,242,320 (Sang Mun So) discloses differently deep trenches formed in a first wafer. A second wafer is also used. The trenches have alternating depths; a deeper trench is positioned between two shallower trenches. By means of two successive polishing steps illustrated in this document in Figs. 26 and 21, cf. column 4, lines 8 to 51, a uniform thickness of the upper wafer is achieved. The trenches are filled with an insulating material, cf. column 3, lines 20 to 29, acting as "polishing stops", associated with an intermediate etch process, in which the deeper trenches (indicated as 25) are etched down to a depth corresponding to the less deep trenches (indicated as 23), cf, Fig. 2H of this document.

[0004] US 6,156,621 (Nance et al., Infineon) discloses a method for manufacturing a Si-Si02-Si wafer, wherein initially isolation trenches (trenches) are provided in a homogeneous silicon wafer that is subsequently bonded with its surface to a second wafer. A conductive layer of polysilicon, indicated as 9 in this document, is located between the 25 two wafers, which fills the trenches and also forms a connecting intermediate layer between the two wafers (indicated as 9, 4). After grinding (thinning)

the front side the isolation trenches may be exposed; the thinning process is performed prior to bonding this wafer to the polysilicon layer in order to form the wafer composite, cf. column 3, lines 18 to 23, or the German counter part DE 197 41 971, column 2, lines 31 to 39. The 30 result is a double wafer including isolation trenches. Due to the influence of the support layer (i.e., the polysilicon layer 4) and to the risk of lattice defects and interferences as well as contaminations of the polished surface during a control measurement monitoring of the grinding and polishing thickness is difficult.

[0005] Depth measurements based on by step structures and conical configurations are disclosed in US 6,514,858 (Hauser et al., AMD), cf. Figs. .$A, 4B and 3C. During the removal process the width of the trenches increases, wherein the filling in was accomplished by means of a metal, which may optically be detected on the basis of its change in width in a step-like or continuous manner. The formation of trenches having a conically configured sidewall structure is technically difficult and is accompanied with an affording necessary measurement procedure on the semiconductor.

[0006] It is an object of the present invention to provide an efficient monitoring and test method, which reduces the failure effects of material removal from wafers, in particular of polishing and lapping. Moreover, costs of the removal process should be reduced by minimizing the complexity of the monitoring as well as resulting refuses, which otherwise may increase costs.

[0007] According to the present invention the object is solved by a test structure (claim 10) used in the context of a method (claim 1). By this (efficient) test structure a system of trenches is determined, which may be used at least for a coarse determination of the amount of removal or removal depth.

[0008] The trenches are disposed in a systematic row. They are provided in a first wafer that is also referred to as device wafer (or active wafer) due to its function of receiving, after the reduction in thickness, active devices such as semiconductors or circuits in one or more later manufacturing processes (claim 5).

[0009] The passive wafer is the carrier wafer, which may be an insulating wafer (claim 6). The two wafers are bonded together by means of a bond connection acting as an area-like connection.

[0010] The systematic row of trenches defines a system of trenches of determined yet

different depth, which are arranged in a sequence. The trenches and their different depths are obtained by etching on the basis of etch mask openings of a mask (claim 3). By means of this etch process trenches of different width and thus different depth (claims 2, 3) are formed in the active wafer. The active wafer later receives the active electronic circuitry, which is the reason for its name.

[0011] The amount or the removal depth during the material removal from the wafer, obtained for instance by polishing or lapping, is controlled on the basis of a desired (target) thickness of the active wafer, which is to be determined in advance (claim 13). When the desired reduction in thickness is achieved the removal process may be terminated (claims 9, 14). In order to detect the end point of the removal process optical means are used for observing the process to monitor the reduction in thickness. To this end, a trench depth is assigned to the target thickness, that is, a trench from the systematic row is selected or determined in advance as a reference trench whose depth at least substantially corresponds to the desired thickness of the active wafer.

[0012] Unless one of the trenches located at the periphery is selected the reference trench is flanked by one less deep (shallower or flatter) trench and one deeper trench. Flanking is to be understood such that the trenches are neighbours of the reference trench, i.e., they are spaced apart yet are located not too far from the reference trench.

[0013] The process of selecting one of the trenches as a reference trench as described above may be performed in a later stage, after the active wafer and the carrier wafer are bonded together. To this end, the trenches are bonded upside down, that is, with their open or upper side facing downwards, onto the surface of the carrier wafer. The top side is the side on which the test structure is located, that is, the surface in which the systematic row of the plurality of trenches has been formed. This side is bonded to the carrier wafer (claim 4).

[0014] When in the process of the wafer treatment the material removal is performed in the active wafer, that is, on the backside of the active wafer, the thickness thereof is reduced. This material removal is continued until the reference trench is visible from the 20 backside of the active wafer, i.e., its bottom is exposed, that is, this trench is visible at all. This is detected by the observation means.

[0015] For detection the removal process may be interrupted and may then, if the

reference trench is not detected by the observation means, continued. This monitoring process may be repeated once or several times until the reference trench is exposed, that is, its bottom is removed by the removal process and thus the reference trench is detected by the optical means.

[0016] By means of a test structure configured in such a manner a determination of thickness during the removal process may be accomplished by an efficient optical, and in particular a visual control. First, the deeper and broader trenches are observed successively during the thinning of the wafer, which may be detected optically.

[0017] The thickness reduction in the vertical direction is thus mapped into a horizontal direction, which may optically detected more efficiently. One obtains a relationship x(t), that is, a distance vs. depth diagram, which exposes increasingly more trenches when the remaining height of the active wafer is continuously being reduced. The removal process is terminated when the reference trench is exposed.

[0018] If, for example, a removal process for exposing one of the trenches of the systematic row previously formed in the active wafer is considered, the test structure may be configured such that the desired depth of the isolation trench of the wafer is located in the central region of the row of the differently deep trenches, i.e., flanked by trenches of less depth and trenches of increased depth (claim 1 , claim 15).

[0019] During the formation of the trenches in the active wafer a respective reference trench of the test structure is formed with the same depth when having the same width as a lo different trench. The broader trenches automatically result in an increased depth during etching, while the narrower trenches result in a reduced depth, cf. US 6,515,826 B1 (Hsiao, IBM), abstract and Figs. 15 and 16, with emphasis on the progression of the trench depth vs. the opening width.

[0020] If two trenches of different width are etched, determined by the etch mask, also trenches o different depth are obtained for identical etch times.

Brief Description of the Figures

[0021] The invention will be explained in more detail on the basis of illustrative embodiments.

[0022] Figure 1 illustrates a test structure in a cross-sectional view. It is shown a cross-section of a row of trenches opened by a removal process and of

trenches still closed when viewed from the (empty) front side of the active wafer of an SO1 wafer assembly. The trenches of reduced depth are still closed.

[0023] Figure 2a is a further embodiment of a portion of the device wafer 2 including a sequence of deep and broad trenches spaced apart from each other.

[0024] Figure 2b is the embodiment of Fig. 2a, bonded to a carrier wafer 1 upside down, wherein the trenches are closed by the bonding process.

[0025] Figure 3a is a top view (when viewed from the removal side 2b") of the sectional view of Fig. 3a.

[0026] Figure 3b is a vertical section corresponding to that of Fig. 1 in a manufacturing stage, in which an increased portion of the first bonded wafer 2 is removed in the height direction so that a greater number of trenches are exposed compared to the embodiment of Fig. 1.

[0027] Fig. 1 is a cross-sectional view. Reference numeral 1 represents an insulating layer, for example, a carrier wafer made of silicon dioxide, $Si0_2$. The active layer 2 is made of, for instance, silicon. It is also referred to as semiconductor layer or device wafer. The top side 2b' of the active layer 2 is depicted in an already thinned state so that three trenches of the plurality of trenches 4, 5, 6, 7, 8, 9 are already opened. The other three trenches are still closed. The wafer has a height h6 that substantially corresponds to the depth of the trench 6 having a width b6. Respective widths b4 to b9 correspond to the trenches 4 to 9, respectively.

[0028] Illustrated in Fig. 1 is the result of the method after performing all of the method steps required for the thinned bonded wafer pair.

[0029] An optical device 30, schematically depicted, is configured to detect open trenches, the bottom sides of which were removed during the removal process, which may be a polishing process or a grinding process or a lapping process. Hereby, the human eye, a technical microscope or a magnifying lens may be used. The removal device, which may be a chemical mechanical polishing tool, in short a CMP, is not shown.

[0030] The entire trench structure as a systematic row of a plurality of trenches forms the test structure. The structure is located in the semiconductor wafer, which may receive

in a later stage an active electronic circuit - also not illustrated - located at a position that does not lie directly in or between the trenches, but that may also be spaced apart therefrom.

[0031] In Fig. 2a there is shown an example of a semiconductor wafer 2 not yet applied to the insulating layer 1 in an upside down configuration is. Here the same trenches as in Fig. 1 are shown that have different width and different depth, while the semiconductor wafer 2 is still thicker. It has a basic thickness ho. Trenches are formed in the semiconductor wafer 2, which form as trenches 4 to 9 a systematic row, ordered by depth and width, wherein during the etch process that is not explicitly shown the broad trenches automatically receive a greater depth as may be appreciated by the skilled person. The trench 4 has the greatest depth and the greatest width. The trench 9 has the smallest depth and the smallest width.

[0032] A respective trench bottom represents the end of the etch process and is indicated for each trench with the reference numeral of the respective trench with an additional letter "a". Thus, 6a is the trench bottom of the trench 6, 7a is the trench bottom of the trench 7.

[0033] Hence, the device wafer 2 has two height sections, that is, the section 2d, in which the trenches are formed, and a further section 2c, which has no trenches formed therein. Both sections are commonly applied to the second wafer 1 of the wafer pair, using the top sides 2a, i.e., the side from which the test structure was formed. This second wafer I may be an insulating layer, formed of, for instance, silicon dioxide. A bonding process is performed in which both wafers are firmly connected to each other.

[0034] The result of the removal of the section 2c of the device wafer is shown in Fig. 1 for the case that the removal was performed to such a depth that ho is reduced to h6 in order to just expose the trench bottom 6a and to make the trench 6 of width 6b visible for the optical device 30. In this state the surface 2b is reduced compared to the remaining surface 2b', as shown in Fig. 1.

[0035] The trench 6 is located substantially in the central region of the row of trenches 4 to 9, so that at both sides thereof trenches are provided, which systematically become deeper and shallower, respectively. From this, a description of a systematic row of trenches results, which has a different depth and is located in the active wafer that is to

receive an active electronic circuit in a later stage. The desired thickness h6 is the target thickness or the target value, to which the thickness is to be reduced. This thickness aimed at as a target value substantially corresponds to the depth t_6 of the trench 6. The more frequently the removal process is interrupted in order to detect the exposure of the reference trench 6 by means of the measurement device 30, the more accurately the removal process may be controlled. Since the reference trench is flanked by at least one deeper trench and at least one shallower trench, that is, these trenches are arranged in parallel, the reduction in thickness with respect to the vertical direction may be mapped to the visible plane.

[0036] The removal process is performed from the opposite side 2b, which is located oppositely with respect to the top side 2a of the formation of the trenches of the test structure.

[0037] The optical device represents a magnifying lens, the human eye or a microscope.

[0038] Fig. 2b illustrates a further embodiment, which shows a perform of the result of Fig. 1. The same reference numerals are used so as to maintain conciseness of the 20 description while nevertheless providing a more detailed understanding. Applying the embodiment of Fig. 2a with its top side 2a to the top side 1 a of the insulating layer 1 yields an SO1 structure with all the trenches 4 to 9 still closed. The respective trenches may become visible upon performing the removal process from the side 2b. The opposing side of the wafer composite formed from bonded wafers is 1b and forms the bottom side for this process step. Here the bonded wafer is supported.

[0039] The height of the device wafer is still ho prior to starting thinning the upper portion 2c of this wafer. The lower portion 2d comprising the trenches in the systematic row is removed only partially to an extent that the reference trench may be detected by the optical device 30.

[0040] By way of example, two reference trenches are indicated as 6 and 7, which shall be separately explained.

[0041] The trenches of different depth of the systematic row represent a gradation of the trench depth and a gradation of the trench width. Trench 6 is deeper and broader compared to trench 7. During the formation of this trench by an etch process using an

etch mask having six openings of different width the trenches as shown are formed.

[0042] Trench 6 is detectable (becomes visible), when the height ho is reduced by the not depicted reduction height by $h_o - t_6$ so that the bottom 6a is removed and the trench is exposed. The optical device 30 may detect this event, when the removal process is discontinued in a temporal neighbourhood with respect to the exposure of this trench and an optical monitoring process is performed intermittently.

[0043] If the trench is not yet visible the removal process may be continued. If the trench is already observable, the removal process may be terminated, as is shown in Fig. 1.

[0044] At reference trench 7 the bottom 7a is concerned, that is, the narrower and less deep trench 7 having the depth t7. When the removal height is increased to $h_o - t_7$, first the trench 6 is exposed, and during the further removal process trench 7 is exposed, too, which may also be detected by the optical device 30.

[0045] A corresponding regime also applies for each of the trenches, for the peripheral trenches 4 and 9 as well, which may also be used for the detection; however, preferably trenches may be used for detection, which are located in the central region of the systematic row of trenches, as is explained above when referring to two removal depths of the alternative reference trenches 6 and 7.

[0046] In a further embodiment of Fig. 3a the device wafer 2, comprised of, for instance, silicon, is depicted in a top view, after a state is reached as is explained with reference to Fig. 2 with respect to the trench 7 and the respective removal depth and removal device.

[0047] All trenches are recognizable as stripe-like trenches each having a length I and a width b. For example, the trench 5 had a length 15, the trench 4 has a width b4. Respective characteristics also apply to all other trenches. The length is greater compared to the width, but in the systematic row the width decreases as the depth of the trenches 4 to 9 should decrease.

[0048] After the removal the surface 2b" is formed, which is scanned by the optical device with respect to visibility of the reference trench 7.

[0049] This state having the removed height h7 of the device wafer 2 is shown in Fig. 3b in a cross-sectional view.

[0050] The lateral direction x maps the depth direction h/t. The more wafer material is removed in the depth direction the more stripes having an increasingly reduced width are formed in the lateral direction x.

[0051] The order of magnitude of the trenches, the trench width, the trench depth and the spacing between the trenches may be tailored according to the requirements of the application.

[0052] Two exemplary configuration sizes may be given, for instance a maximum trench width of 5 μm for the broadest and deepest trench 4, and a gradation of, for instance, 0.5 μm with respect to the trench width and thus the trench depth. As a pattern for spacings between the trenches a measure of, for instance, 10μm may be recommended. The trenches may be positioned such that the form a fixed pattern with different widths, which may correspond in electronic applications to pulse width modulation that is here applied to the trench width in a systematic row of trenches of different sizes.

[0053] The trenches may be filled with an insulating material or a conductive material, such as silicon dioxide and polysilicon, respectively, instead of being unfilled. The optical device may be configured to optically distinguish the different materials, for instance by reflection, by colour or based on material composition.